REMARKS

Claims 1-29 are pending in the application. Claim 24 has been amended. No new matter has been added.

Applicants respectfully submit that the present application is now in condition for allowance. Accordingly, reconsideration and allowance of the present application are respectfully requested.

Claim Objections

The Office Action objects to claim 24 because of an informality in the claim.

Claim 24 has been amended to address such informality.

Reconsideration and withdrawal of the objection are respectfully requested.

Claim Rejections – 35 U.S.C. §102

The Office Action rejects claims 1-3, 7-8, 10-12, 15-21 and 24-29 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,218,742 to Carlton et al. ("Carlton").

Reconsideration and withdrawal of the rejections are respectfully requested.

Claim 1

Independent claim 1 recites a device that includes a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal. The device further includes a ring

counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal.

Carlton does not teach or suggest the device of independent claim 1.

Carlton discloses a system for controlling a serial data channel with a microprocessor (title). The system includes a VFO 51 and a clock generator circuit 52 (FIG. 2; col. 3, lines 41-46). A squelch signal initiates operation of the VFO at its free running frequency (col. 3, lines 64-66). The clock generator 52 may include a suitable bit ring counter and other suitable circuitry (including a clock control unit 60, a sync byte detector 62) (FIG. 2; col. 3, line 66-col. 4, line 2). The output of the sync byte detector 62 is supplied to the clock control unit 60 (FIG. 2). The output of the clock control unit 60 is supplied to the bit ring counter (FIG. 2), which also receives the output of the VFO (FIG. 2; col. 3, line 66-68). The function of the sync byte detector 62 is to recognize a sync byte or some other special character which is recorded on a track (col. 4, lines 11-15). On detecting the special pattern, the clock controls are set to control the bit ring clock (col. 4, lines 19-21). See also, col. 4, lines 7-10, the clock controls are turned on by the signal from the sync byte detector 62 and turned off by the disable SBD signal at BR7 time.

However, Carlton does not teach or suggest a device that includes the combination of (1) a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal and (2) a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal, as recited in independent claim 1.

Notably, the sync byte detector 62 and the clock control unit 60 do not appear to synchronize a signal with the output of the VFO 51. For that matter, the sync byte detector 62 and the clock control unit 60 do not even receive the output of the VFO 51. Therefore, even if the sync byte detector 62 and the clock control unit 60 constitute a synchronization circuit, as asserted in the Office Action, and even if the output of the VFO 51 constitutes a clock signal, as asserted in the Office Action, the asserted synchronization circuit does not synchronize a signal with such clock signal. Indeed, the asserted synchronization circuit does not even receive such

clock signal. Moreover, because the asserted synchronization circuit does not synchronize a signal with the clock signal, the asserted synchronization circuit cannot possibly generate a load signal based on such synchronized signal. Still further, because the asserted synchronization circuit does not generate a load signal based on such synchronized signal, the bit ring counter cannot receive such a load signal from the asserted synchronization circuit. Consequently, even if the bit ring counter constitutes a ring counter, as asserted in the Office Action, the asserted ring counter does not receive such a load signal from the asserted synchronization circuit.

Thus, Carlton does not teach or suggest the apparatus of independent claim 1.

Independent claim 1 should therefore be allowed.

Claim 10

Independent claim 10 recites a method that includes receiving a synchronization signal, the synchronization signal substantially synchronized with a data transition; synchronizing the synchronization signal with a clock signal; generating a load signal based on the synchronized synchronization signal, the load signal including a load pulse; inputting the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to a minimum data transition period; and outputting the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the data transition period.

Carlton does not teach or suggest a method that includes receiving a synchronization signal, the synchronization signal substantially synchronized with a data transition; synchronizing the synchronization signal with a clock signal; generating a load signal based on the synchronized synchronization signal, the load signal including a load pulse; and inputting the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to a minimum data transition period, as recited in independent claim 10. Nor does Carlton teach or suggest a method that further includes outputting the load signal from a first node of the ring counter, a period

between successive outputs of the load pulse being substantially equal to the data transition period, as recited in independent claim 10.

Thus, Carlton does not teach or suggest the method of independent claim 10.

Independent claim 10 should therefore be allowed.

Claim 19

Independent claim 19 recites a device to receive a synchronization signal, the synchronization signal substantially synchronized with a minimum data transition period; synchronize the synchronization signal with a clock signal; generate a load signal based on the synchronized synchronization signal, the load signal including a load pulse; input the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to the minimum data transition period; and output the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the minimum data transition period.

Carlton does not teach or suggest a device to receive a synchronization signal, the synchronization signal substantially synchronized with a minimum data transition period; synchronize the synchronization signal with a clock signal; generate a load signal based on the synchronized synchronization signal, the load signal including a load pulse; and input the load signal into a ring counter of one or more delay elements, a time for the load pulse to propagate completely through the ring counter being substantially equal to the minimum data transition period, as recited in independent claim 19. Nor does Carlton teach or suggest a device to further output the load signal from a first node of the ring counter, a period between successive outputs of the load pulse being substantially equal to the data transition period, as recited in independent claim 19.

Thus, Carlton does not teach or suggest the device of independent claim 19.

Independent claim 19 should therefore be allowed.

Claim 28

Independent claim 28 recites a system that includes a memory controller hub including a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal. The memory controller hub further includes a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal, and a parallel-to-serial converter to generate serial data based on the load signal. The memory controller hub further includes a double data rate memory to receive the serial data.

Carlton does not teach or suggest a system that includes a memory controller hub including the combination of (1) a synchronization circuit to receive a synchronization signal, the synchronization signal substantially synchronized with a data transition, to synchronize the synchronization signal with a clock signal, and to generate a load signal based on the synchronized synchronization signal and (2) a ring counter to receive the load signal from the synchronization circuit and to circularly propagate the load signal, as recited in independent claim 28. Nor does Carlton teach or suggest (3) that the memory controller hub further includes a parallel-to-serial converter to generate serial data based on the load signal and (4) that the system further includes a double data rate memory to receive the serial data, as recited in independent claim 28.

Thus, Carlton does not teach or suggest the system of independent claim 28.

Independent claim 28 should therefore be allowed.

Dependent claims

Claims 2-9, 11-18, 20-27 and 29 depend from independent claims 1, 10, 19 and 28, respectively, and therefore should be allowed for at least the reasons set forth above with respect to independent claims 1, 10, 19 and 28, respectively.

CONCLUSION

For at least the reasons set forth above, Applicants respectfully submit that the present application is in condition for allowance. Accordingly, reconsideration and allowance of the present application is respectfully requested.

Because the reasons set forth above are sufficient to overcome the rejections set forth in the outstanding Office Action, Applicants do not address some of the assertions set forth therein and/or other possible reasons for overcoming the rejections. Nonetheless, Applicants reserve the right to address such assertions and/or to present other possible reasons for overcoming the rejections in any future paper and/or proceeding.

If the Examiner believes that a telephone interview would expedite the prosecution of this application in any way, the Examiner is cordially requested to contact the undersigned via telephone at (203) 972-0006, ext. 1014.

Respectfully submitted,

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